

# COSY-3D – EURIPIDES 07-302 Compact Secure SYtem in 3D

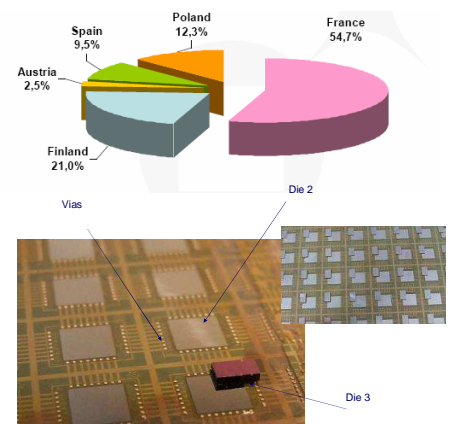
## Objectives :

- Collaboration with industrial, research centres and academia to create an innovative, **highly secure and portable intelligent system**, for
  - **advanced telephony,**
  - **multimedia,**
  - **secure transactions,**
  - **enterprise access (digital & physical).**

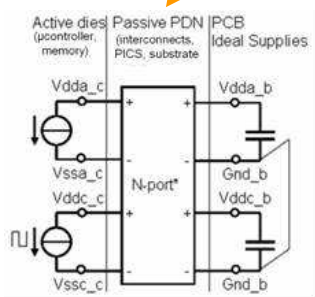


## Solutions:

- **Structured 3D system** which will enable the functions of Memory & CPU,
- **Stable MEMs** based Oscillator/Resonator,(48MHz)
- **Passive Components** and some RF blocks to be **integrated** into the smallest possible footprint block.
- All of these components will be integrated in a vertical manner at Wafer Level ; **“Front Side Connected Die Stacking”**
- ➔ and will exhibit very short, vertical low capacitance interconnections with associated performance improvements over more conventional MCM approaches.

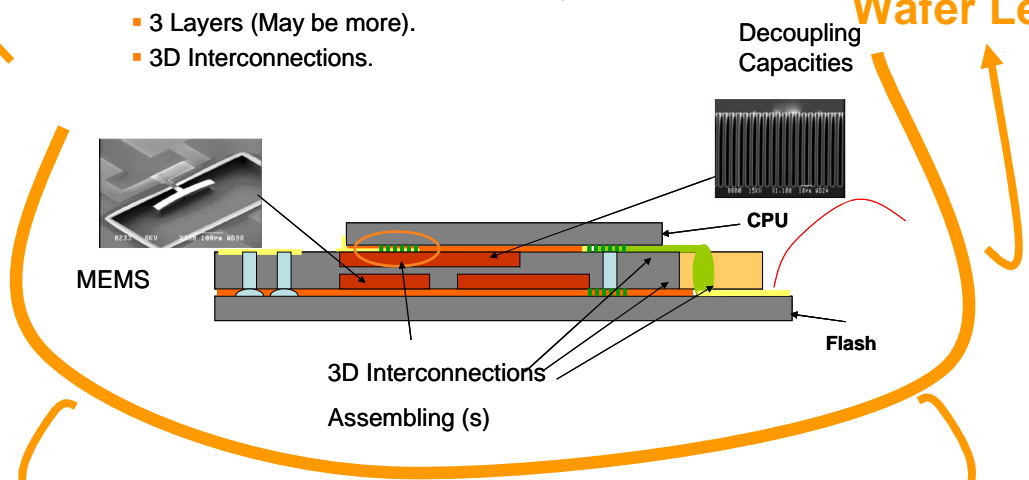


## Design and Simulation



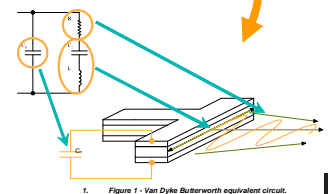
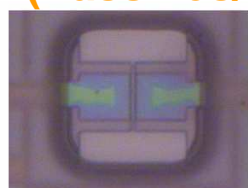
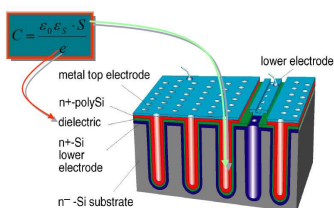
- 3 Dies, ie: Flash / “multi-function” component / CPU.
- 3 Layers (May be more).
- 3D Interconnections.

## Integration Wafer Level



## Component Development (Passives/Clock)

The World Record of Capacitance Density on (in?) Silicon



1. Figure 1 - Van Dyke Butterworth equivalent circuit.

