PIDEA+ 04.160 “Sm@rtPack”

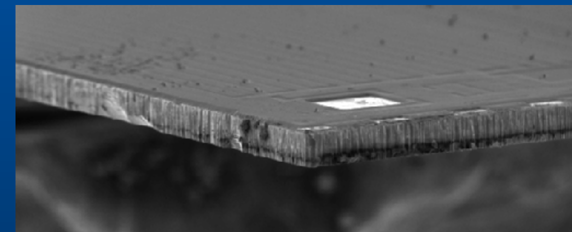
Berlin 2nd Euripides Forum

Project Frame

- Eureka (Σ!) PIDEA+ project 04.160
- Supported by the Public Authorities of
  - Austria, Finland, France
- Budget & Timeframe
  - 9.2 M€ for 50.3 P*Y, May 2005 - May 2008
- Partners
  - In France: AXALTO [PL], ATMEL, CEA-LETI
  - In Austria: Datacon, EVG, Philips
  - In Finland: SETEC, VTT
    - AXALTO and SETEC now in Gemalto
    - Philips now NXP

Project Goals

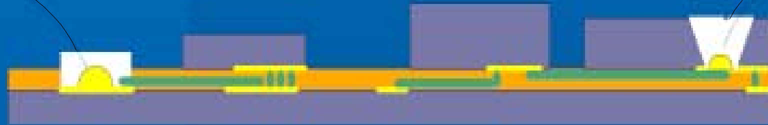
- Smart Card packaging with 2 axis:
  - Chip stacking
  - Contactless Assemblies
- Background
  - **WALPACK** (PIDEA 01.131) Gemalto, Leti
    - Thinning, dicing, bonding, encapsulation
    - Ultra thin wafer handling
  - **ACSIP** (PIDEA 00.127) Gemalto, Leti
    - Secure solutions for specific markets
      - Wafer level assembly and thinning
  - **FLEXI** (Σ!) Datacon, Philips
  - **Vertical System Integration** (FP6) Datacon, Philips

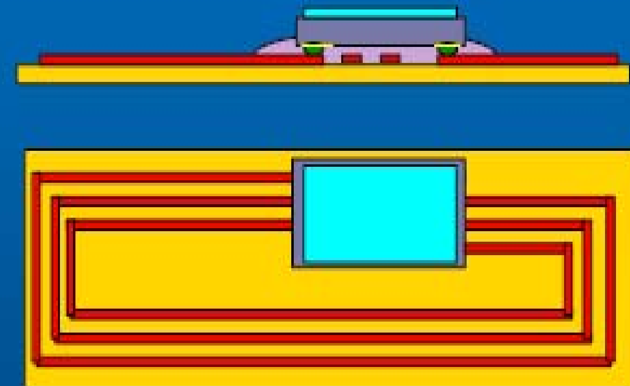


Sm@rtP@ck: what is it?

Stacking Die to wafer Module

Contactless





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Contactless Assemblies

- Propose a very thin C'less card
- Why
  - Passport & E-Visa
  - For ID and Access Control markets
- Objectives
  - Inlay thickness < 100 µm
  - High reliability (10 yrs)

Chip Stacking

- Enhance current SC functionalities
- Why:
  - Low cost, high security, high yield
  - Second sourcing
  - Short Time To Market
- How
  - By stacking peripherals on the µP

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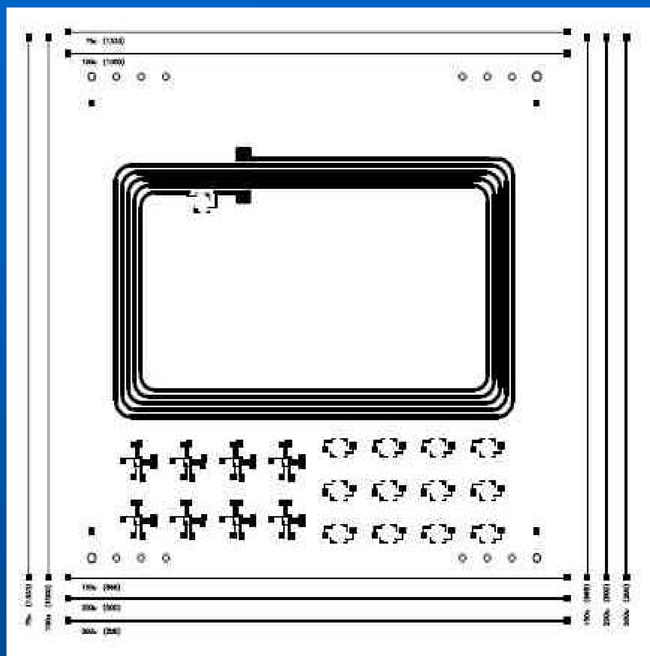
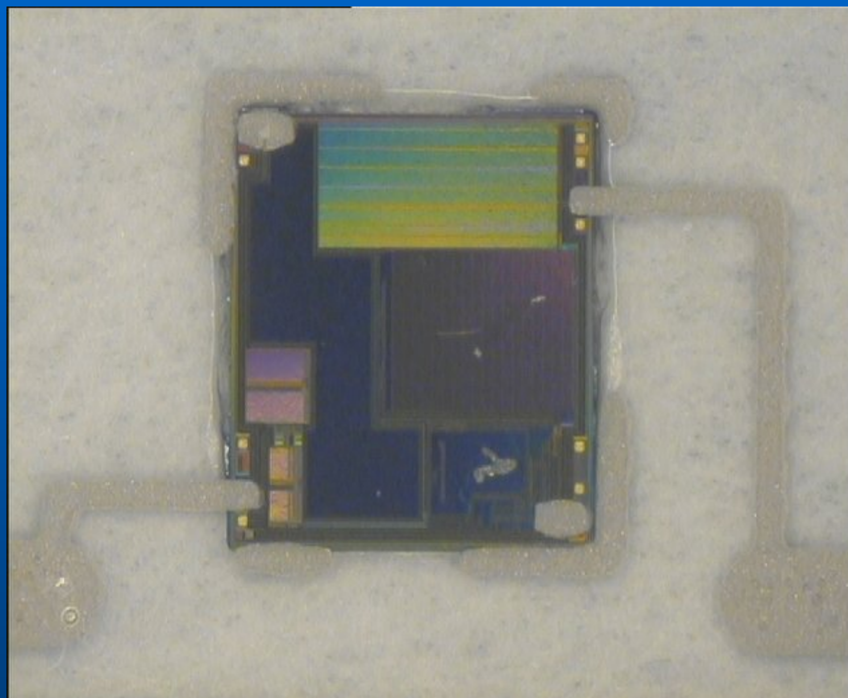
C'Less ; Antennas made at VTT



2.9 x 3.2 mm 75 μm thick
Microprocessor from NXP
18 μm Au bumps



The chip interconnections
seen through the flex

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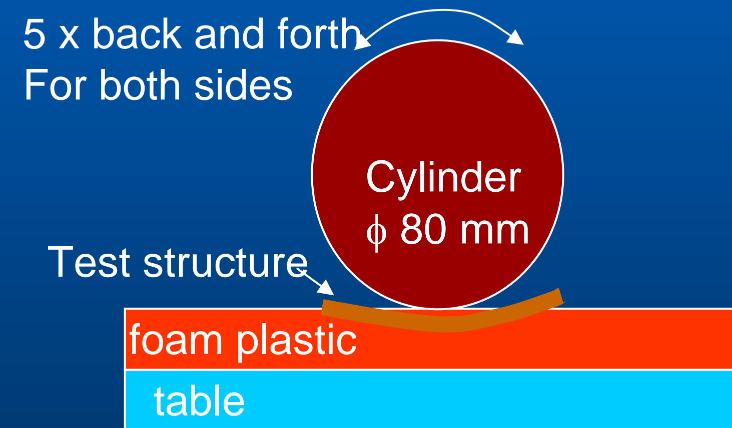
C'Less ; Preliminary reliability tests

- LETI dummy chips, ISIT test chips, functional antennas
- Initial measurements: Resistance measurements for dummy test chips and functional testing for the antenna structures
- Thermal cycling in ESPEC Mini-subzero MC-811
  - 32 … + 77 °C
  - cycle 85 min, dwell time 10 min
  - 50 + 50 cycles
- Measurements after 50 and 100 cycles
- Bend testing
- Measurements
- Thermal humidity testing 85 °C / 85% RH 116 hours
- Final measurements



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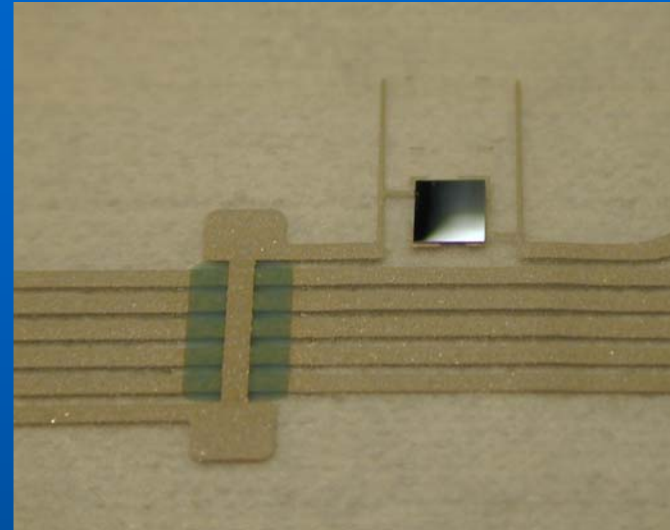
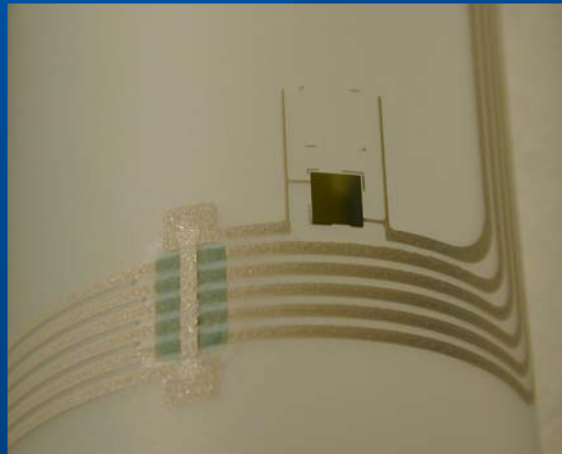
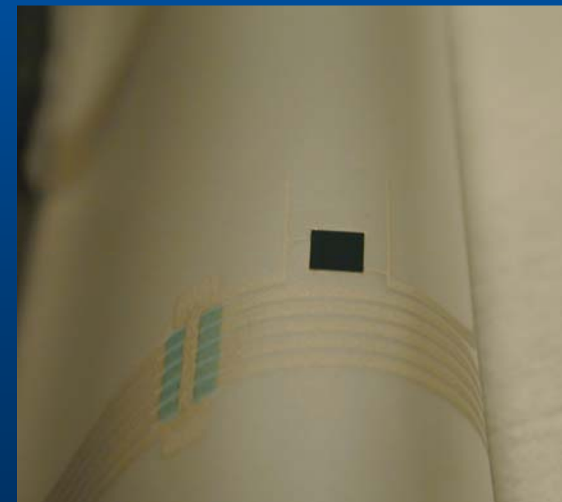
Smartpack Contacless Demonstrators





Chip 75µm

PC 100µm

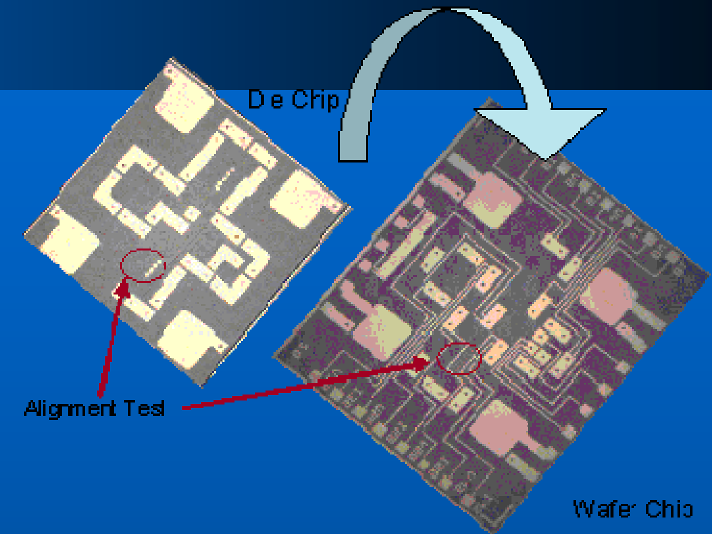


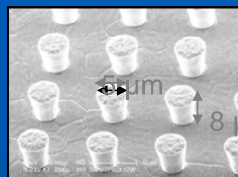
Chip 50µm

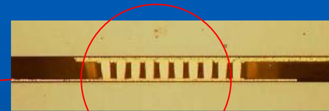
PC 30µm

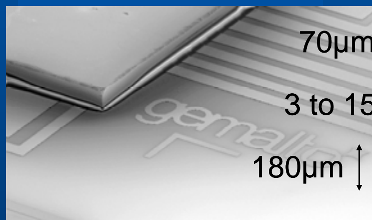
Stacking results

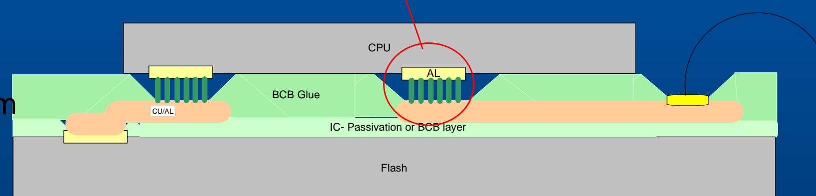
- On Test Vehicle Technology Validation
  - Yield
  - Reliability (T Cycling /Humidity)

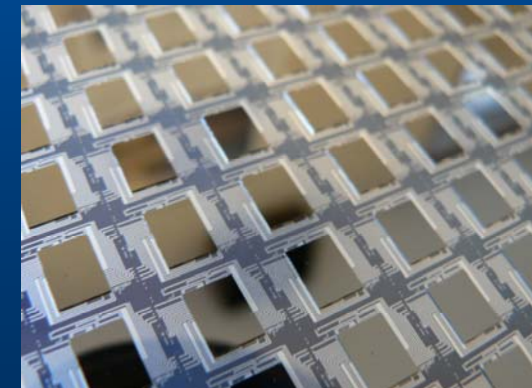












- µinsert Technology
- RDL at the Interface
- Wafer Level Polymerization

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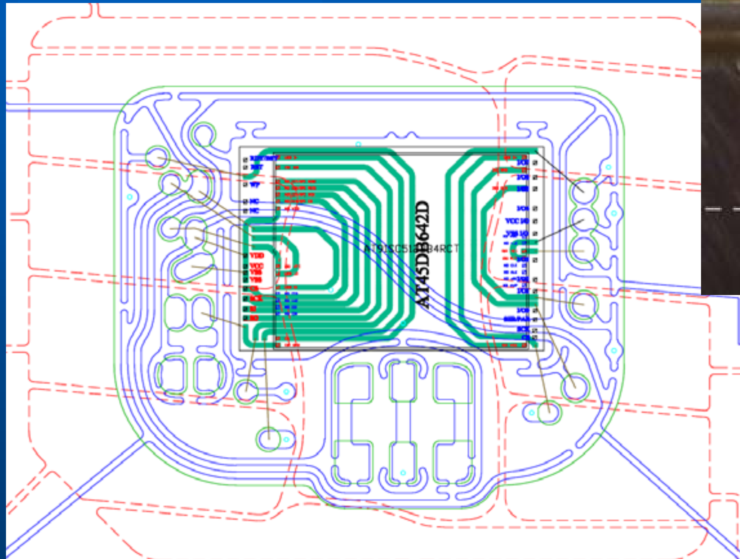
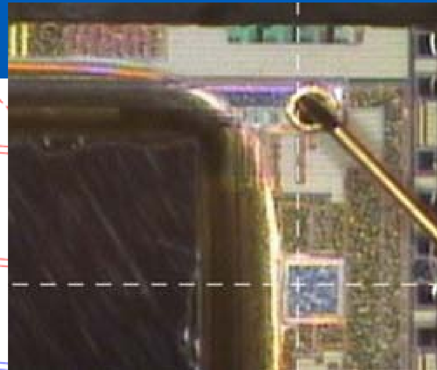
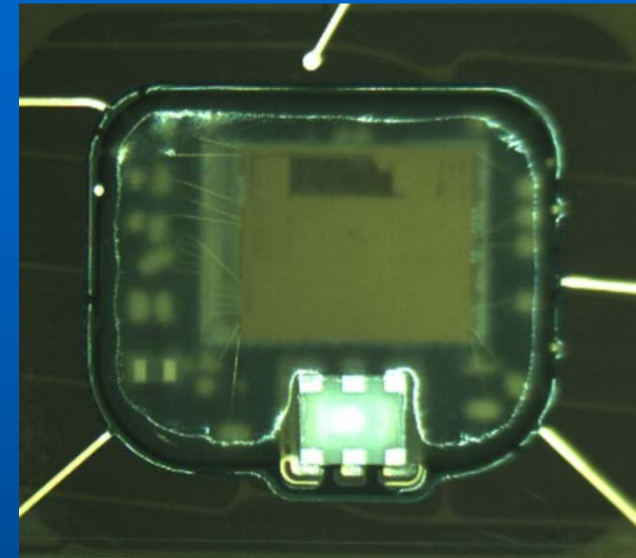
Stacking Results ; Demonstrator

NOR Flash memory AT45DB642D
µProcessor AT91SC512384RCT
(Comm protocol = ISO + SPI + USB)







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Smartpack Stacking Conclusions

- First functional prototypes were done without any specific problem during assembly step. Wire bonding on the metallization added by LETI was within the specification.

- Some adhesive flowing of the adhesive on the flash pads have been observed and prevent any wire bond on the chip.

- Global yield obtained during the manufacturing was 67% (both protocol ISO & USB). Integrating defect units with USB, seems to be due by the resonator frequency.

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